REMARKS

The claims are claims 1, 3 to 5, 16, 18, 19, 21 and 25 to 33.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. These amendments include a SUMMARY OF THE INVENTION that was originally omitted.

Claims 1, 3, 8, 19, 21, 25, 26 and 27 are amended. Claims 2, 6 to 15, 17, 20 and 22 to 24 are canceled. New claims 30 to 33 are added. Claim 1 is amended to recite subject matter previously recited in canceled claim 2 with additional clarity. Claim 3 is amended to depend upon claim 1 rather than canceled claim 2. Claim 18 is amended to present better form. Claim 19 is amended to recite subject matter previously recited in canceled claim 20 with additional clarity. Claim 21 is amended to depend upon claim 19 rather than canceled claim 20. Claim 25 is amended to present better form. Claims 26 and 27 are amended like the amendments to claim 19. New claims 30 to 33 recite that the trace information, the timing information and the temporal information is formed into fixed length packets.

Claims 1, 16, 18, 19, 25 and 26 were rejected under 35 U.S.C. 102(b) as anticipated by Edwards et al U.S. Patent No. 6,918,065. Claims 2 and 20 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards et al U.S. Patent No. 6,918,065 and Bellamy "Digital Telephony", 1982, John Wiley & Sons.

Claims 1, 19 and 26 recite subject matter neither anticipated by Edwards et al nor made obvious by the combination of Edwards et al and Bellamy. Claims 1, 19 and 26 recite "said timing information including cycle bits each indicating whether the data processor performed data processing operations or stalled during a corresponding clock cycle." This recitation corresponds to the teaching of the application at page 17, lines 15 to 29 and

illustrated in Figure 4. Note Figure 4 refers to the timing information as "cycle bits." Edwards et al states at column 8, lines 39 to 44:

> "Pre-scaler **216** provides an increment signal to a reference counter **217** which generates a reference count from a predetermined time. Reference counter **217** may provide an absolute count of time to trace processor **205** for preparing timestamp information."

Thus Edwards et al teaches a timing count rather than an indication of whether a data processor operated or stalled as claimed. Bellamy likewise fails to teach information where bits indicate whether a data processor operated or stalled on a corresponding cycle. Accordingly, claims 1, 19 and 26 are allowable over Edwards et al and the combination of Edwards et al and Bellamy.

Claims 1, 19 and 25 recite further subject matter neither anticipated by Edwards et al nor made obvious by the combination of Edwards et al and Bellamy. Claim 1 recites "inserting...in the timing stream temporal information indicative of a temporal relationship between the trace information and the timing information." Claims 19 and 26 recite "timing generator operable when trigged by said trigger signal to insert temporal information corresponding to said next sync ID number from said table into the timing stream." The OFFICE ACTION cites Edwards et al at: Figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 23, lines 23 to 30; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value" as anticipating this limitation. The portions of Edwards et al cited in the OFFICE ACTION teach insertion of a timestamp or similar data into the emulation information stream. These portions of Edwards et al fail to teach any insertion of information into the timing stream as recited in claims 1, 19 and 26. Figure 8 of this application shows a connection between ID NUMBERS 83 and TIMING PACKET GENERATOR 81

which enables this claimed insertion. In contrast, Figure 2 of Edwards et al illustrates no such connection to reference counter 217. Accordingly, Edwards et al fails to anticipate the recited insertion into the timing stream. Accordingly, claims 1, 19 and 26 are allowable over Edwards.

Claims 19 and 26 recite still further subject matter not anticipated by Edwards et al. Claims 19 and 26 each recite "a table of sync ID numbers" and that the insertion is of "said next sync ID number from said table." The Applicant respectfully submits that Edwards et al includes no teaching of any such structure. Accordingly, claims 19 and 26 are allowable over Edwards et al.

Claims 3 to 5 and 21 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards et al, Bellamy and Goldrian et al "Tracing of Large Amounts of Data by Using Main Memory as a Trace Buffer", IBM Technical Disclosure Bulletin, Volume 40, Number 6, June 1997.

Claims 3 and 21 recite subject matter not made obvious by the combination of Edwards et al, Bellamy and Goldrian et al. Claims 3 and 21 recite "wherein said inserting step includes inserting mutually corresponding identifiers in both the trace stream and the timing stream." This recitation requires insertion into both the trace stream and the timing stream. The OFFICE ACTION cites Edwards et al at: Figure 2, elements 218, 216, 217, 205, 221, 203, 204, 202; and column 23, lines 23 to 30; and column 13, Table 1, field "Timestamp"; and column 23, Table 7, field "Time Value" as anticipating this limitation. The portions of Edwards et al cited in the OFFICE ACTION teach insertion of a timestamp or similar data into the emulation information stream. These portions of Edwards et al fail to teach any insertion of information into the timing stream as recited in claims 3 and 21. Accordingly, claims 3 and 21

are allowable over the combination of Edwards et al, Bellamy and Goldrian et al.

Claims 4, 5, 16, 18, 21, 28 and 29 are allowable by dependency upon allowable base claims.

Claims 30 to 33 recite subject matter neither anticipated by Edwards et al nor made obvious by the combination of Edwards et al, Bellamy and Goldrain et al. Claims 30 to 33 recite that the stream of trace information, the stream of timing information and the temporal information are formed of fixed length packets. Fixed length information blocks are disclosed in the application at page 21, line 14 to page 26, line 6 which describe an example 10-bit format. Edwards et al discloses variable length fields. The trace message fields of Table 1 include a variable length (1, 2, or 4 bytes) program counter field. The trace message fields of Tables 2 and 3 include a variable length (0 or 1 bytes) timestamp field, a variable length (0 or 1 bytes) ASID and a variable length (1, 2, or 4 bytes) program counter field. Accordingly, claims 30 to 33 are allowable.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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